Amendments to the Drawings

The attached sheets of drawings includes changes to Figs. 3, 5 and 6. In Figs. 3, 5 and 6, additional reference numerals are added to further clarify the invention.

REMARKS

Initially, in the Office Action dated January 10, 2005, the Examiner objects to the drawings, specification and claims because of informalities. Claims 1-11 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over JP 05159080 (Takahashi et al.) in view of U.S. Patent No. 6,078,623 (Isobe et al.).

By the present response, Applicant has submitted new claim 12 for consideration by the Examiner and respectfully submit that this claim does not contain any prohibited new matter. Further, Applicant has amended claim 1 to further clarify the invention. Claims 1-12 remain pending in the present application.

Information Disclosure Statement

The Examiner indicates that the Information Disclosure Statement filed on 9/4/2001 does not fully comply with the requirements of 37 C.F.R. §1.98. Applicant is submitting concurrently with this response an IDS that complies with all USPTO requirements.

Drawing Objections

The Examiner has objected to Figs. 3, 5 and 6 as not showing reference characters described in the specification. Applicant has amended the figures and/or the specification of the present application to further clarify the invention and respectfully request that these objections be withdrawn.

Specification Objections

The disclosure of the present application has been objected to because of informalities. Applicant has amended the specification to further clarify the invention and respectfully request that these objections be withdrawn.

Claim Objections

Claims 1-11 have been objected to because of informalities. Applicant has amended the claims of the present application to further clarify the invention and respectfully request that these objections be withdrawn.

35 U.S.C. §112 Rejections

Claims 1-11 have been rejected under 35 U.S.C. §112, second paragraph. Applicant has amended the claims of the present application to further clarify the invention and respectfully request that these rejections be withdrawn.

35 U.S.C. §103 Rejections

Claims 1-11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al. and further in view of Isobe et al. Applicant respectfully traverses these rejections.

Takahashi et al. discloses a technique for designing a clock distribution system that easily makes a clock skew be a minimum where the circuit is designed by dividing a semiconductor chip into a plurality of blocks of which area are mostly equal to one another, respectively, individually providing the clock distribution system including clock input terminals, buffer circuits and phase adjusting circuits for respective blocks and providing the clock distribution system in the shape of a tree

for the respective blocks so that the wiring between respective nodes are equal in length and capacitance. Consequently, as the semiconductor is divided into the plurality of blocks, the wiring length from the clock input terminals to flip-flops, etc., at ends become short so that the wiring designation of the equal length and capacity becomes easy and a clock delay time from input terminals to the end circuits become short so that the absolute value of clock can be reduced.

Isobe et al. discloses a transmission apparatus capable of transferring data between a transmitting and a receiving device using a small-scale, low-cost hardware implementation for high-speed data transmission, the apparatus being conducive to reducing the amount of system design work on a target system. The transmitting device sends to the receiving device both data and a reference signal generated by a reference signal generation circuit. On the receiving side, a phase adjustment circuit delays the reference signal and a phase determination/phase amount control circuit brings the delayed signal into phase with a receiving-side clock signal. A data signal group is given the same amount of delay as the reference signal. The scheme allows data signals to be received directly in keeping with the receiving-side clock signal, eliminating the need for strict clock skew management, massive detours of data transmission lines or a wasteful wait time required for signal values to be established.

Regarding claim 1, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of this claim of, inter alia, a semiconductor integrated

circuit that includes a first circuit block, a second circuit block, a first signal path, a second signal path, a first buffer circuit and a second buffer circuit where the circuit blocks, the first and second signal paths, and the first and second buffer circuits are formed on a single semiconductor substrate, or where the clock signal and the data signal are transmitted in parallel to each other on the first and second signal paths, and the data signal is taken by the second circuit block by the clock signal. The Examiner admits that Takahashi et al. does not disclose or suggest details of the clock and data transmission paths between the different blocks as recited in the claims of the present application, but asserts that Isobe et al. discloses these limitations. Specifically the Examiner appears to assert that Isobe et al. discloses a clock signal and a data signal being transmitted in parallel with each other on the first and second signal paths, and the data signal being taken by the second circuit block by the clock signal, in Fig. 13, block 92, 90 and 91, and col. 13, lines 46-47. However, these portions of Isobe et al. merely disclose a block diagram of a data transmission facility to implement full-duplex data transmission using two printed circuit boards 19, 29, and the transmission lines 90-92 between the two printed circuit boards. This is not circuit blocks, first and second signal paths, and first and second buffer circuits being formed on a single semiconductor substrate, as recited in the claims of the present application. Isobe et al. does not disclose or suggest anything related to a semiconductor integrated circuit. Isobe et al. teaches away from the limitations in the claims of the present application in that it discloses two printed circuit boards and transmission lines between the printed circuit boards. This

is not circuit blocks and signal paths formed on a single semiconductor substrate. Moreover, this is not a semiconductor integrated circuit wherein a clock signal and a data signal are transmitted in parallel to each other on the first and second signal paths and the data signal is taken by the second circuit block by the clock signal, as recited in the claims of the present application.

Moreover, the Examiner asserts that Isobe et al. discloses at least a first buffer circuit connected to a first signal path in such a manner as to constitute the first signal path and at least a second buffer circuit connected to the second signal path in such a manner as to constitute the second signal path at Fig. 13, blocks 92-16-26 and blocks 91-3, and col. 13, lines 62-65. However, as noted previously, these portions of Isobe et al. merely disclose two printed circuit boards and the transmission lines between the two printed circuit boards. This is not a first buffer circuit constituting a first signal path and a second buffer circuit constituting a second signal path, the first and second buffer circuits placed between the first and second circuit blocks and formed on a single semiconductor substrate, as recited in the claims of the present application. These portions of Isobe et al. merely disclose logic gates on one printed circuit board and phase amount adjustment groups on a second separate printed circuit board.

Further, Applicants submit that there would be no motivation to combine Takahashi et al., which relates to reducing clock skew on a semiconductor chip, with Isobe et al., which relates to a data transmission apparatus including two circuit boards that "eliminates the need for strict clock skew management . . . " (see,

Abstract). These two references present different solutions for a problem in two different environments. Takashi et al. relates to a semiconductor chip, whereas in contrast, Isobe et al. discloses two circuit boards. One of ordinary skill in the art would have no motivation to combine these two references since their techniques are for different environments and are in contrast with each other. Moreover, this combination fails to achieve the limitations in the combination of each of the claims of the present application.

Regarding claims 2-11 and new claim 12, Applicant submits that these claims are dependent on independent claim 1 and, therefore, are patentable at least for the same reasons noted previously regarding this independent claim. For example, Applicant submits that none of the cited references disclose or suggest wherein said second circuit block includes a plurality of circuits operated in synchronism with the internal clock generated based on the clock signal received from said second signal path, and said clock distribution line pattern of said second circuit block is configured to distribute said internal clock to said plurality of circuits through the substantially same length of path; or wherein said second circuit block includes a phase shifting circuit for generating a clock signal out of phase by one half period of the data transmission cycle based on the received clock, and a phase adjusting circuit for generating a clock signal giving a timing of taking data to said holding means based on the clock signal generated by said phase shifting circuit, and wherein said phase adjusting circuit operates to adjust the phase of the clock signal supplied to said holding means in such a manner that the clock signal generated by said phase-

shifting circuit is in phase with the phase of the clock signal supplied to said holding means; or wherein said holding means is configured to take said received data signal substantially at the center between the changing points of said received data signal; or wherein the first buffer circuit is placed in a predetermined length of the first signal path, and the second buffer circuit is placed in said predetermined length of the second signal path.

Accordingly, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of each of claims 1-11 and new claim 12 of the present application. Applicant respectfully requests that these rejections be withdrawn and that these claims be allowed.

In view of the foregoing amendments and remarks, Applicant submits that claims 1-12 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 500.40612X00).

Respectfully submitted,

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Attachment: Replacement Sheets